JOURNAL OF MATERIALS SCIENCE **34** (1999) 4711–4717

Silicon-to-indium tin oxide coated glass bonding for packaging of field emission arrays fabricated on silicon wafer

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A silicon-to-In_2O_3:Sn coated glass bonding has been developed for the package of field emission arrays fabricated on the silicon wafer, utilizing a conventional silicon-to- silicon anodic bonding using the glass layer. A 1.8 μm Pyrex #7740 glass layer was deposited on the In_2O_3:Sn coated glass by an electron beam evaporation. It was confirmed that the composition of the glass layer was nearly the same as that of the bulk Pyrex #7740 glass plate. In this work, bonding the silicon and In_2O_3:Sn coated glass was achieved at a temperature of 190 °C with an applied voltage of 60 V_{dc}. A secondary ion mass spectroscopy analysis was used to confirm the modeled bonding kinetics of the silicon-to-In_2O_3:Sn coated glass.

1. Introduction

The anodic bonding technique has been widely employed in the manufacture of microsensors and micromechanical devices [1–5]. The anodic bonding is a very promising technique because of the relatively low temperature required, simple bonding process, and high hermetic sealing capability [6–9]. Many processes have been developed for silicon-to-bulk glass bonding or silicon-to-silicon bonding using the glass layer since its development by Wallis and Pomerantz in 1969 [10–14].

The most popular material used in anodic bonding is a Pyrex #7740 glass, which contains enough sodium ions for the bonding process in addition to well-matched thermal expansion coefficient to the silicon wafer. The Pyrex #7740 glass has a small amount of sodium oxide (Na_2O), and the sodium atoms can be easily ionized at room temperature. At an elevated temperature, the sodium ions become quite mobile and can be transferred by an external electric field.

Flat panel displays (FPDs), such as an field emission display (FED) [15], are currently attracting a lot of attention. FED devices have many potential advantages, including high brightness and resolution, wide viewing angle and operating temperature range, and compatibility with established integrated circuit (IC) processes [16]. FED devices consist of two glass plates. A luminescent phosphor coating is applied to the lower surface of a face plate and field emission arrays (FEAs) of metal or semiconductor tips are fabricated on the higher surface of a base plate. FEAs are also commonly fabricated on a silicon wafer using IC fabrication processes. The silicon wafer is generally attached to the base glass plate using an indium paste for the conventional packaging of FED devices. A vacuum packaging of FED devices is currently performed in a manner analogous to that used for a cathode ray tubes (CRT) [17]. The two plates are aligned and held together with a solder glass frit which is placed between the plates in the peripheral edge-sealing area, then the plates are heated up to 450 °C. At this temperature, the glass frit material melts, sealing the two plates together. But during the packaging process, the indium paste also melts and contaminates FED devices. Therefore, a solid state attaching method is needed for the packaging of FEAs fabricated on the silicon wafer.

In this work, we anodically bonded a silicon wafer and an In_2O_3:Sn coated glass substrate at a low temperature and voltage using a glass thin film deposited by an electron beam evaporation, and investigated the role of sodium ions for the silicon-to-In_2O_3:Sn coated glass bonding using a secondary ion mass spectroscopy (SIMS) analysis. Finally, a packaging method of FEAs fabricated on the silicon wafer was proposed using this bonding method.

2. Experiments

A 1.8 μm thick glass layer was prepared by an electron beam evaporation technique on the front glass

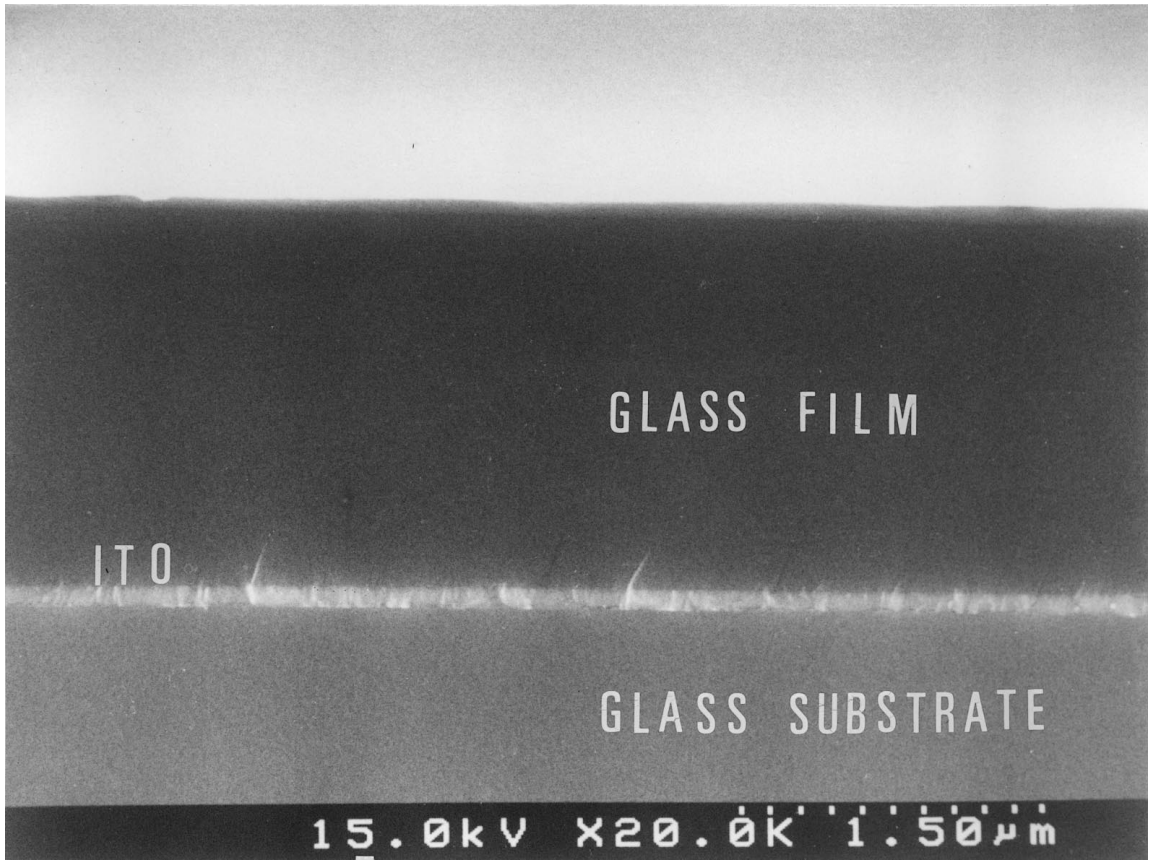

Figure 1 Cross-sectional SEM photograph of glass layer deposited on ITO coated glass substrate.

substrates coated with a transparent electrode indium tin oxide (ITO:Sn-doped In_2O_3), which has a sheet resistance of about 20 Ω/□ (Fig. 1). The glass layer was deposited at a substrate temperature of 230 °C. The base pressure in the chamber was adjusted to 2×10^{-5} Torr and the pressure during the deposition was maintained at 5×10^{-5} Torr. Pyrex #7740 glass was used as the source material for the electron beam evaporation.

Auger electron spectroscopy (AES) analysis was adopted to characterize the film composition according to their deposition methods. To investigate the variation of the surface roughness, an atomic force microscope (AFM) analysis was performed for the ITO and glass layer deposited on the glass substrate coated with the ITO.

In the bonding procedure, 5 cm × 5 cm × 0.5 mm Si (100) n-type wafers and 7 cm × 6 cm × 1.1 mm ITO coated glass substrates were used. The assemblies were placed on specially designed field-assisted bonding equipment (Fig. 2). The bonding process was performed at a temperature of 190 °C with an electrostatic voltage of 60 V_{dc}. A negative voltage was applied to the ITO layer so that the glass layer is negative with respect to the silicon wafer. The applied voltage was kept for 10 min to allow the bonding current to settle at a steady-state leakage current.

TABLE I Composition of glass layer and bulk glass plate

	Materials		
Elements (%)	Bulk glass	Glass thin film deposited by electron beam evaporation	Glass thin film deposited by sputtering
Si	23.70	25.90	21.36
O	68.56	69.69	74.30
B	7.74	4.41	4.34

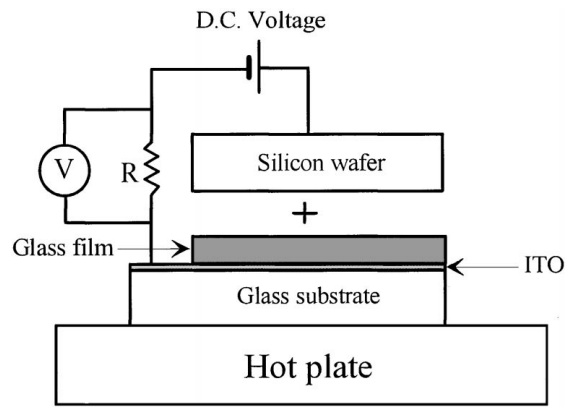

Figure 2 Schematic experimental setup for silicon-to-ITO coated glass bonding.

3. Results and discussion

Results from the AES analysis are summarized in Table I. It was confirmed that the composition of the glass layer deposited by the electron beam evaporation is nearly the same as that of the bulk Pyrex #7740 glass plate, whereas the glass layer deposited by a radio-frequency magnetron sputtering method has a different composition compared with the bulk glass plate. The physical properties, such as the thermal expansion coefficient, are greatly affected by changes in composition

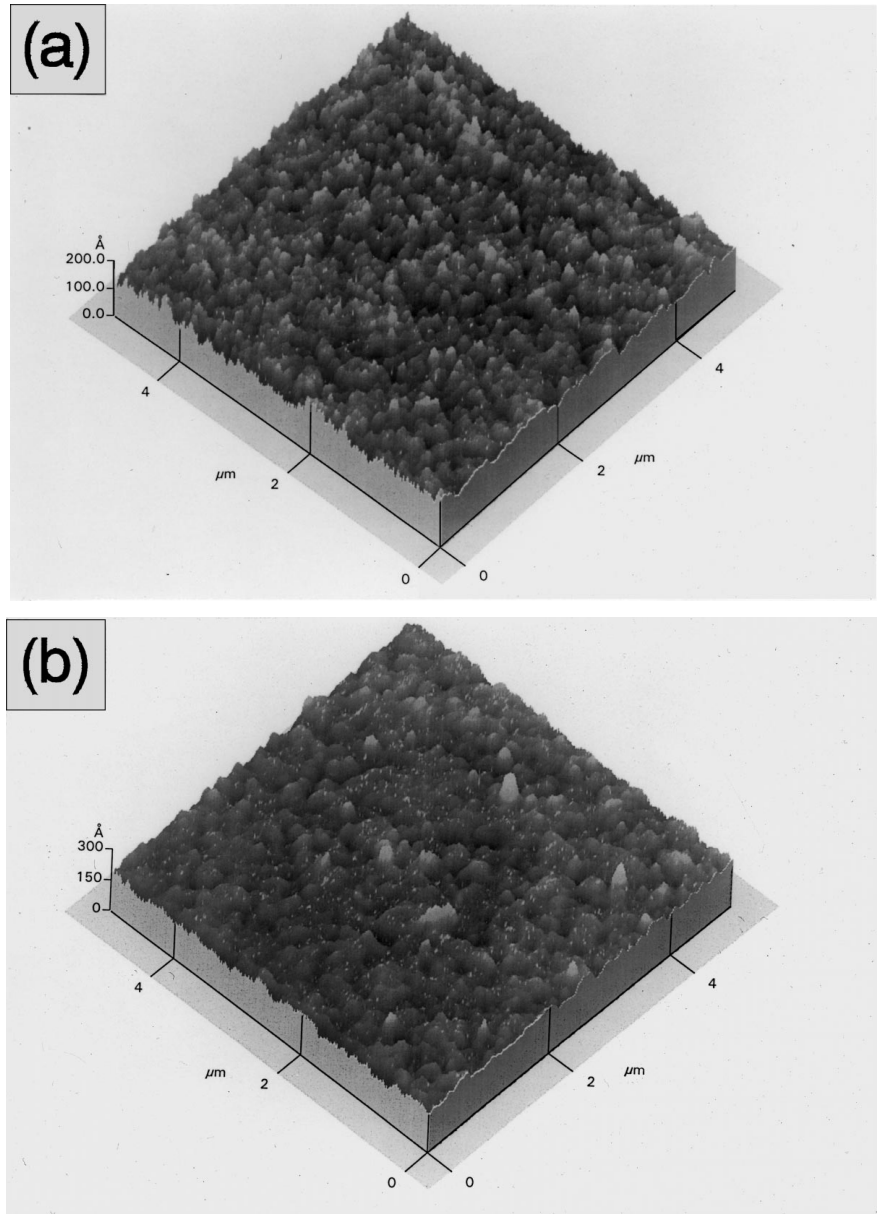

Figure 3 AFM photographs of surface roughness: (a) ITO layer; (b) glass layer deposited by electron beam evaporation.

[18]. The more same composition can lead to the more same physical properties.

In the anodic bonding procedure, the surface roughness of specimens is one of the most critical bonding parameters. The significant effect of the rough surface is seen by a decrease in the bonding strength or even by the failure of bonding. Fig. 3 shows AFM images of the ITO and glass layer. It was revealed that the roughness of the glass layer was slightly increased, compared with the glass substrate coated with the ITO layer. The surface roughness of the glass layer is less than 200 Å peak-to-valley and the ITO layer 150 Å.

When an external voltage is applied at an elevated temperature, the positive sodium ions are attracted toward the ITO layer, leaving more fixed negative oxygen ions in the surface region of the glass layer. A sodium-depleted layer is formed in this region adjacent to the bare silicon to be sealed. As a result, a space charge region is formed at the interface between the glass layer and the silicon wafer, where most potential drop occurs. In this case, the glass layer and the silicon act as a parallel capacitor. The resulting large electrostatic force pulls the negative ions in the glass layer from the bulk to the surface and forms Si─O─Si bonds.

In order to characterize the bonding process, a current-time characteristic was measured during the bonding process. Bonding process was performed at a temperature of 190 °C with an electrostatic voltage of 60 V_{dc} for 10 min. The bonding current rapidly decayed and then remained at its minimum level, as presented in Fig. 4. The obtained current density profile was well fitted with the typical current-time relationship in the anodic bonding process, which describes the transport properties of the sodium ion. Therefore, the capacitive current observed during the bonding process may be attributed to the transport of the sodium ion in the glass layer. To investigate the thermal compatibility of silicon to ITO coated glass bonding during annealing at 450 °C for the packaging process of FED device, the thermal shock testing was performed on the sample bonded at 190 °C. When the sample was heated up to 500 °C and cooled down to room temperature, no difference could be observed. This result shows that the specimen bonded at 190 °C is strong enough to attach FEAs to the

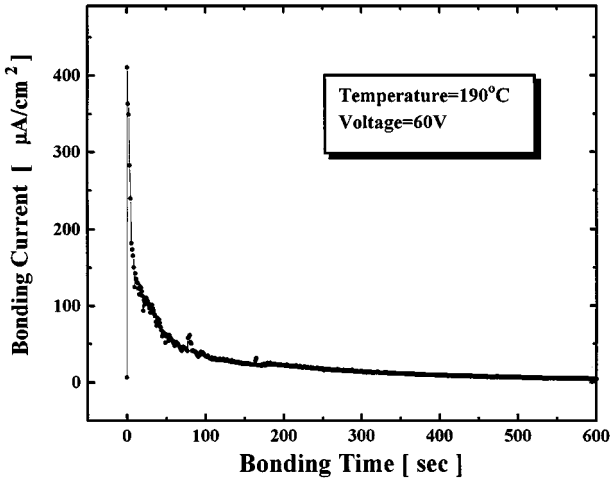

Figure 4 Typical current density versus time relationship during bonding process.

base glass plate during the packaging process. And the bonding process below 200 °C is required to prevent the surface oxidation of field emission tips which causes the bad effect on the field emission characteristic.

When the pull tests were performed to measure the tensile strength, fractures appeared at the bulk of the silicon wafer or the interface between the silicon wafer and the glass layer. It was also observed that the glass layer was partly removed from the ITO coated glass substrate on which they were originally deposited and found on the surface of the silicon to be sealed. This result indicates that the bond strength is higher than the adhesion of the glass layer to the ITO coated glass substrate. Fig. 5 shows the change of the glass layer after the bonding process. The region A is the area where the bare silicon was not contacted and no change occurred. On the other hand, the region B is the area where the bare silicon was contacted and the silicon-to-ITO coated glass bonding was performed. The glass layer was partly removed from the ITO coated glass by the pull test.

To study the role of the sodium ion in the bonding mechanism, the SIMS analysis was carried out on the regions A and B from the glass layer to the ITO layer, respectively. The SIMS spectra are shown in Fig. 6a for

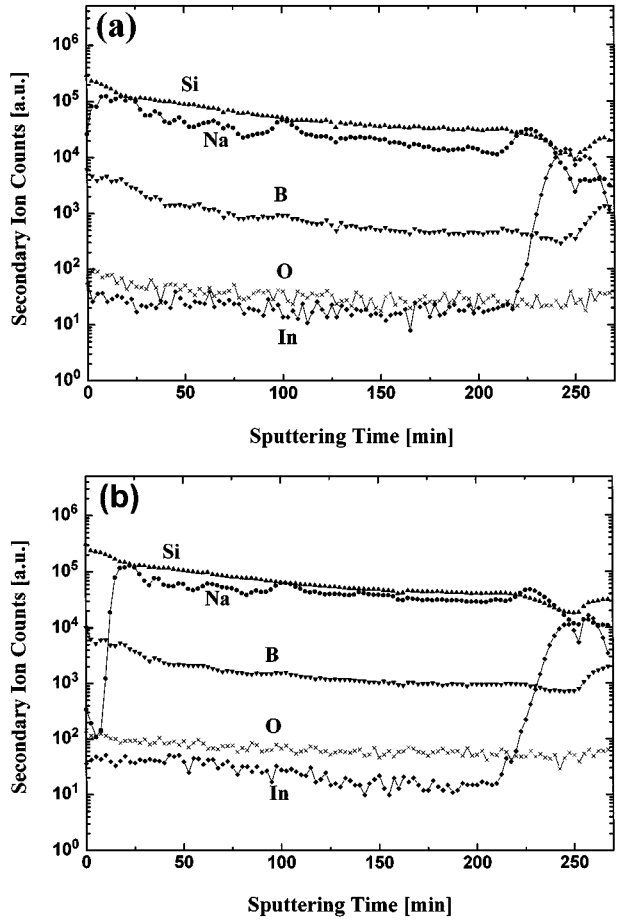

Figure 6 Depth profile of region A and B: (a) depth profile of region A where the sodium ions are almost uniform; (b) depth profile of region B where the sodium ions are depleted from the surface. The thickness of the sodium-depleted region is about 150 nm.

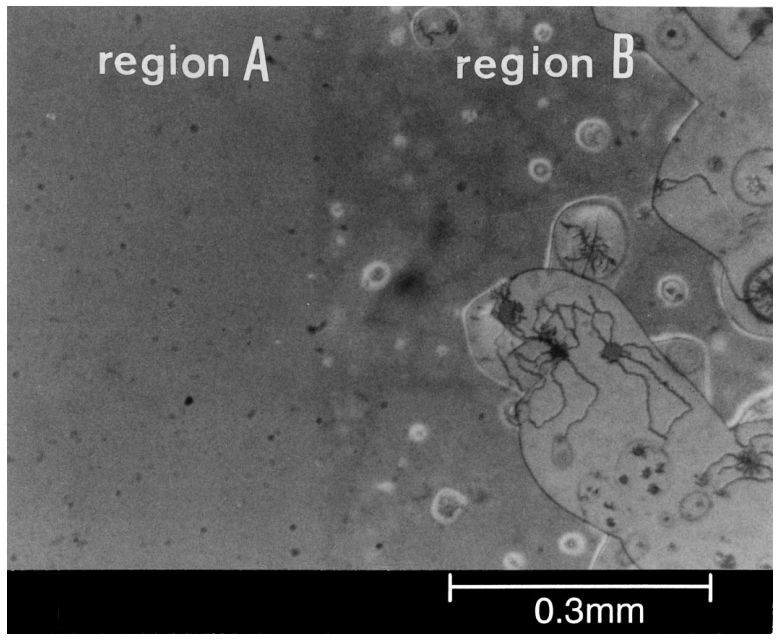

Figure 5 Optical microscopic photographs of glass layer surface after pull test.

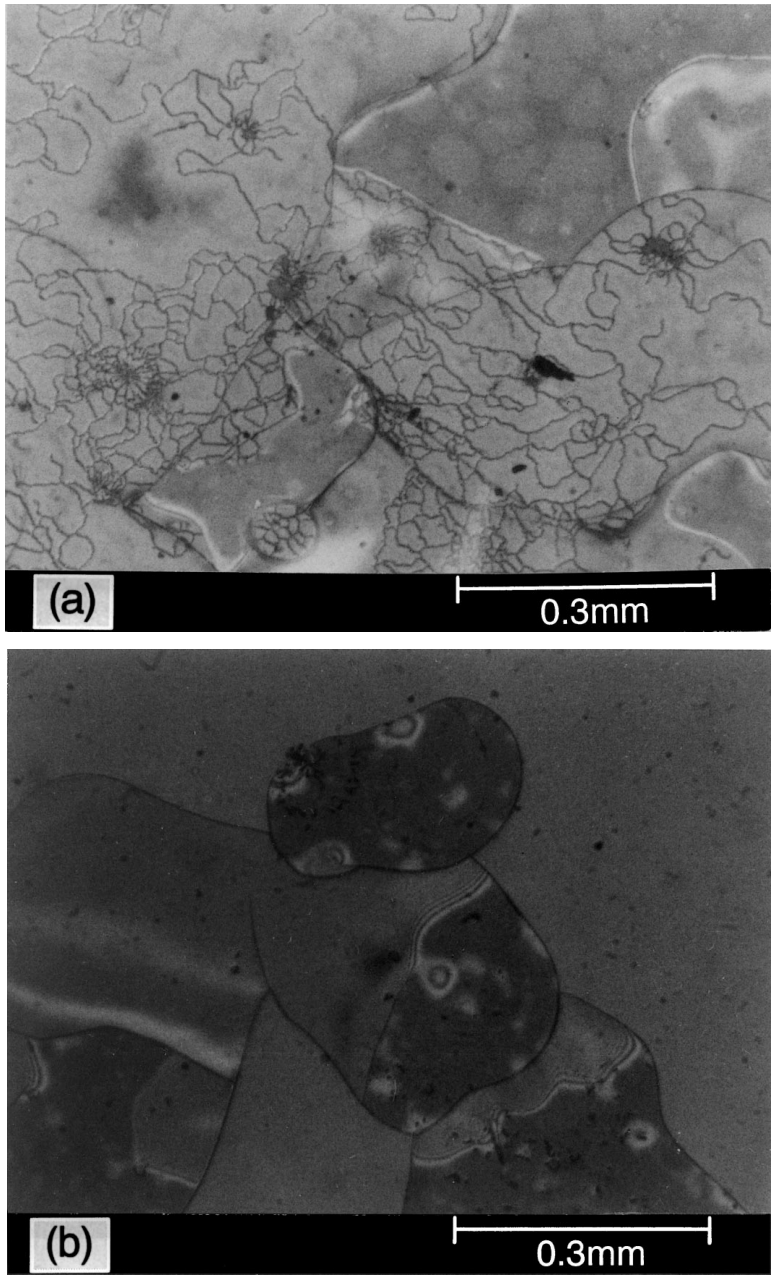

Figure 7 Optical microscopic photographs of ITO coated glass substrate and bare silicon to be sealed after the pull test: (a) ITO coated glass; (b) bare silicon to be sealed.

the region A and in Fig. 6b for B. From the spectra, it is evident that the most significant feature is formed by the difference of the depth profile of the sodium ion. On the other hand, no difference was found for the other atoms. The sodium ions are uniform in the region A, whereas they are almost depleted from the surface of the region B. This is in agreement with the theoretical bonding model. As refereed to the sputtering rate of 100 Å/min during the SIMS analysis, the thickness of the depletion region is estimated as about 150 nm.

In order to investigate the variation of the morphology after the pull test, the optical microscopic photographs were taken for the ITO coated glass substrate and the bare silicon to be sealed, as shown in Fig. 7. It can be easily observed that the glass layer was partly removed from the ITO coated glass substrate. In Fig. 7a, the cracked region indicates the area where the glass layer was removed. Here, it is pointed out that the glass layer removed from the ITO coated glass is found on the surface of the bare silicon to be sealed.

The bonded specimens were cut to investigate the bonded interface region of the silicon-to-ITO coated glass substrate assembly. Fig. 8 shows the cross-sectional photograph of a scanning electron microscope (SEM).

4. Conclusion

A silicon-to-ITO coated glass substrate boning was performed using the anodic bonding process. Pyrex #7740 glass was deposited on the ITO coated glass substrate by an electron beam evaporation. Using AES analysis, it was confirmed that the composition of the glass layer was nearly the same as that of the bulk Pyrex #7740

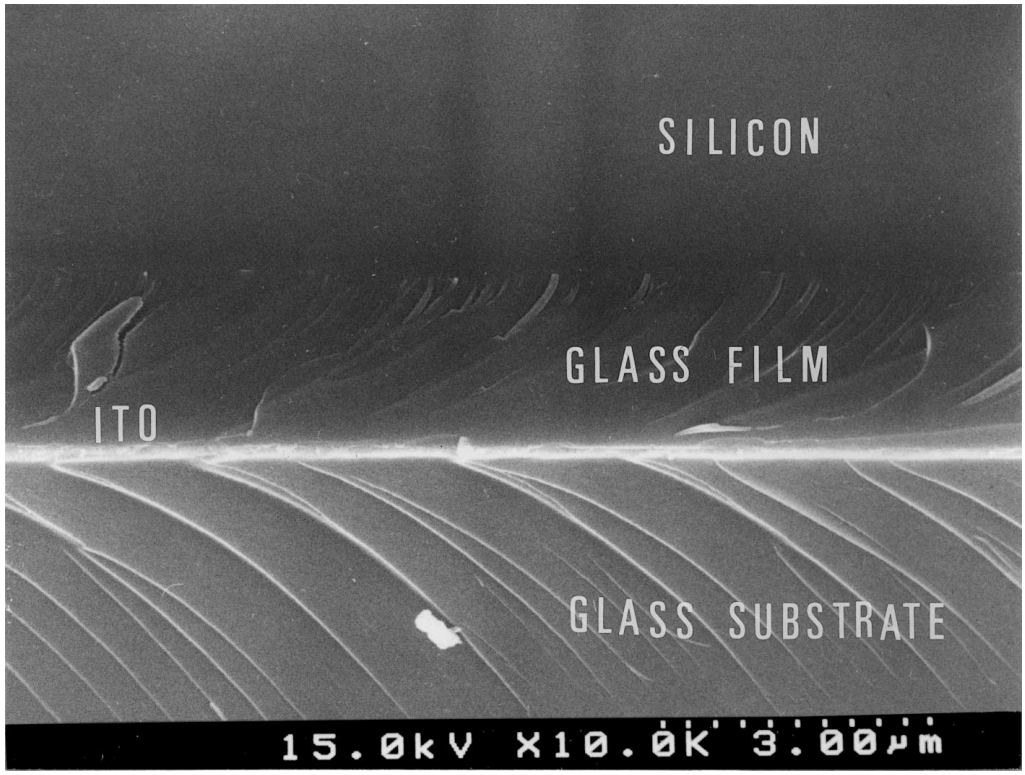

Figure 8 SEM photograph of boded interface region of silicon-to-ITO coated glass assembly.

glass plate. Bonding the silicon and the ITO coated glass substrate was achieved at a temperature of 190 °C with an applied voltage of 60 V_{dc}. A theoretical analysis in conjunction with SIMS results enabled determining the role of the sodium ion in the silicon-to-ITO coated glass bonding mechanism.

This bonding method can be applied to attach FEAs fabricated on the silicon wafer to the base glass plate. Using FEAs attached on the ITO coated glass plate, it is possible to apply the commercial vacuum packaging process for FED devices to FEAs fabricated on the silicon wafer (Fig. 9).

Acknowledgements

The authors would like to thank Dr. Byungwhan Kim with Center for Information and Communications at Korea University for his continuous help and useful discussions in preparing this manuscript. This work was supported by the Korean Ministry of Trade, Industry and Energy.

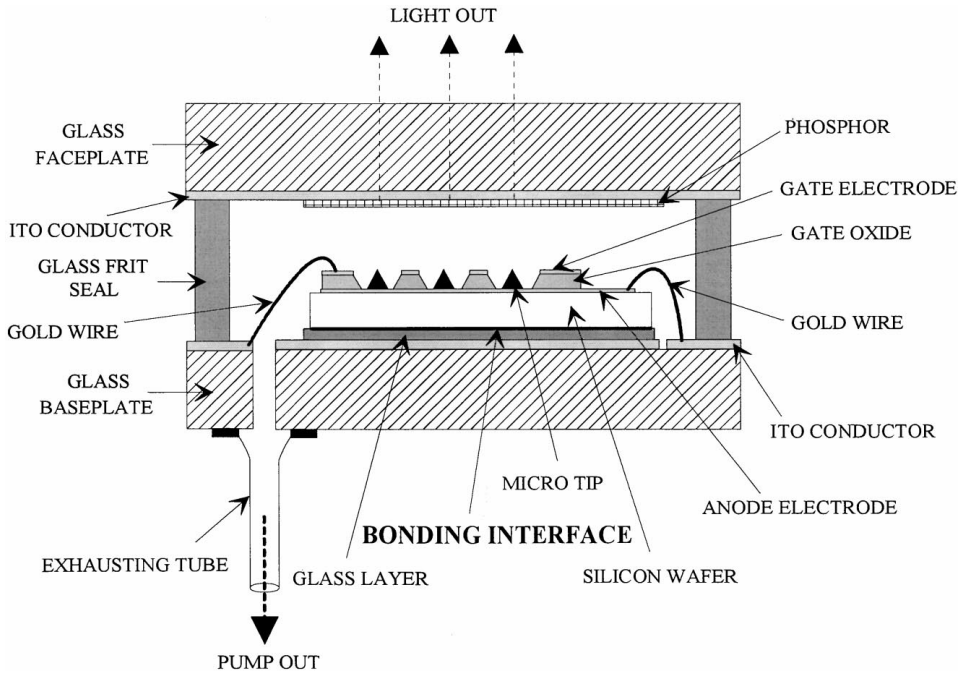

Figure 9 Vacuum packaging method of FEAs fabricated on silicon wafer using silicon-to-ITO coated glass bonding.

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Received 9 September 1998
and accepted 3 March 1999